AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-21 (Cancelled)

22. (Currently Amended) An array substrate for in-plane switching mode liquid crystal display device, comprising:

a substrate having a plurality of pixel regions;

a [[plurality of]] gate line [[lines]], a gate electrode, a [[plurality of]] common line [[lines]] and a common electrode on the substrate;

a first insulating layer over the substrate;

a semiconductor layer on the first insulating layer;

a [[plurality of]] data line [[lines]], source and drain electrodes and a pixel electrode on the substrate including the semiconductor layer, the pixel electrode and the common electrode in each pixel region, the common line and the pixel electrode [[being formed]] forming a first storage capacitor;

a second insulating layer over the substrate;

an auxiliary line on the second insulating layer and [[being overlapped with]] overlapping the common line, the pixel electrode and the auxiliary line [[being formed]] forming a second storage capacitor; and

a dummy line in a non-display area of the substrate,

wherein the dummy line [[communicates with]] is connected to the auxiliary line.

23. (Previously Presented) The array substrate according to claim 22, wherein the dummy line includes one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W),

molybdenum (Mo), copper (Cu) and chromium (Cr).

24. (Previously Presented) The array substrate according to claim 22, wherein the auxiliary line includes one of Indium-Tin-Oxide (ITO) and Indium Zinc Oxide (IZO).

25. (Previously Presented) The array substrate according to claim 22, wherein the gate line, the common line and the common electrode are formed using the same material on a same layer.

26. (Currently Amended) The array substrate according to claim 22, wherein the gate line, the common line and the common electrode [[includes]] include one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

27. (Currently Amended) The array substrate according to claim 22, [[further comprising]] wherein the first an insulating layer is between the common line and the pixel electrode to form [[a]] the first auxiliary storage capacitor.

28. (Currently Amended) The array substrate according to claim 27, wherein the first insulating layer includes one of silicon nitride (SiNx) and silicon oxide (SiO_2).

29. (Currently Amended) The array substrate according to claim 22, [[further comprising an]] wherein the second insulating layer is between the pixel electrode and the auxiliary line to form [[a]] the second [[auxiliary]] storage capacitor.

30. (Currently Amended) The array substrate according to claim 29, wherein the second insulating layer includes one of silicon nitride (SiNx) and silicon oxide (SiO_2).

31. (Currently Amended) The array substrate according to claim 22, wherein [[the]] a thin film transistor [[having a]] includes the gate electrode, [[an active layer]] the semiconductor layer, [[a]] the source electrode and [[a]] the drain electrode.

Claims 32-39 (Cancelled)